VOLTAGE SUPPLY DISTRIBUTION ARCHITECTURE FOR A PLURALITY OF MEMORY MODULES

Field of the Invention

[0001]   The present invention relates to electronic circuits, and, more particularly, to a power voltage supply distribution architecture for a plurality of memory modules. More specifically, the invention relates to an architecture for distributing supply voltages to a plurality of memory modules supplied through a plurality of charge pump circuits.

Background of the Invention

[0002]   By way of example, the present is particularly well suited (though not exclusively) to an architecture for distributing supply voltages to a plurality of Flash memory modules. The following description is provided with reference to this field of application for clarity of illustration only.

[0003]   A Flash non-volatile memory requires a plurality of voltages, which are generated from a same supply voltage reference Vdd. In particular, to correctly perform the different operations (reading, programming, and erasing) on Flash memory cells, some voltages among the plurality of voltages need to have a higher value than the supply voltage Vdd, while other voltages need to have negative values. That is, these

are values lower than a ground voltage reference GND, corresponding to a zero or null voltage value.

[0004]   To increase memory performance, the memory may be split into several banks or modules, and the above-noted operations (i.e., reading, programming, and erasing) are performed in parallel on different banks. Memory architectures capable of performing a reading operation on different banks are known in the art. Examples of such memory architectures are described in U.S. Patent Nos. 5,691,955 (assigned to Mitsubishi Electric) and 5,684,752 (assigned to Intel).

[0005]   Memory architectures capable of performing reading and programming operations in parallel are also known, and examples thereof are described in U.S. Patent Nos. 5,245,572 (assigned to Intel) and 5,867,430 to Chen et al., for example. The memory architecture described in the Chen et al. patent is also capable of performing reading and erasing operations in parallel as well.

[0006]   Such architectures may have certain limitations. First, it may not be possible to perform programming and erasing operations in parallel. Moreover, these architectures are not capable of managing more than two parallel operations. Additionally, these architectures are not capable of managing requests from a number of banks that is different from the number contemplated during the design of the architecture, unless the hardware structure of the architecture itself is changed.

Summary of the Invention

[0007]   The technical problem underlying the present invention is to provide an architecture for

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distributing supply voltages to a non-volatile memory. More particularly, the memory may be of the Flash type and organized in memory modules capable of generating different voltages needed for the correct operation of the memory itself. Moreover, this is to be done while ensuring total parallelism between the reading, programming and erasing operations to be performed on memory cells, as well as the correct management of a plurality of requests coming from different memory modules, to thus overcome the limitations currently affecting the architectures according to the prior art.

[0008]   The present invention provides an architecture for distributing supply voltages to a plurality of memory modules including a block for generating the voltages required for the correct operation of the memory. This block is physically and functionally separated from a block for managing the requests received from the banks included in the memory.

[0009]   The above-noted technical problem is solved by an architecture as described and defined in Claim 1, below.

Brief Description of the Drawings

[0010]   The various features and advantages of the architecture according to the present invention will be further understood from the following description of an embodiment thereof, which is given by way of non-limiting example, with reference to the attached drawings, in which:

[0011]   FIG. 1 is a schematic block diagram illustrating a memory device including an architecture for distributing supply voltages to a plurality of

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memory modules in accordance with the present invention; and

[0012]   FIG. 2 is a schematic block diagram illustrating in greater detail the architecture for distributing supply voltages of FIG. 1.

Detailed Description of the Preferred Embodiments

[0013]   With reference to FIG. 1, a Flash non-volatile memory device 1 including a memory section 2 organized in banks or memory modules Mod1, … ModN is first described. In the illustrated example, the Flash memory section 2 includes the four memory modules Mo1, …, Mod 4 which are connected to a supply voltage reference Vdd. The Flash memory device 1 also includes a voltage generator block 3.

[0014]   As mentioned above with reference to the prior art, for the correct operation of Flash memory modules it is necessary to generate a plurality of voltages Vhigh1, …, VhighN with a higher value than the supply voltage reference Vdd, as well as a plurality of negative value voltages Vneg1, …, VnegN. It should be noted that for generating these supply voltages Vhigh1, …, VhighN and Vneg1, …, VnegN, a plurality of charge pump circuits Pump1, …, PumpM included in the voltage generator block 3 are generally used. Each charge pump is capable of supplying a predetermined amount of current.

[0015]   In accordance with the invention, the memory device 1 advantageously includes an arbitrator block 10 inserted between the charge pump circuits Pump1, …, PumpM of the voltage generator block 3 and the plurality of memory modules Mod1, …, ModN. More

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particularly, the block 10 is connected to the voltage generator block 3 through a first bi-directional bus 5, and to the Flash memory section 2 through a second bi-directional bus 6.

[0016]   The block 10 advantageously receives a plurality of requests for supply voltage values (herein "power requests") from the memory modules. The block 10 conveniently drives the charge pump circuits Pump1, …, PumpM of the voltage generator block 3 to ensure correct values for the supply voltages Vhigh1, …, VhighN and Vneg1, …, VnegN sent to the plurality of memory modules Mod1, …, ModN. The block 10 therefore provides an architecture for distributing supply voltages generated by the plurality of charge pump circuits for the plurality of memory modules during the different operating steps of the memory device.

[0017]   Turning now additionally to FIG. 2, the architecture 10 illustratively includes a sorting block 11 which is input-connected to the second bi-directional bus 6, from which it receives a power request signal PSreq from a memory module of the plurality of modules. The second bi-directional bus 6 may also include an identification bus PSidfy for identifying the operation required, and a priority bus PSrqpry for the request signal PSreq.

[0018]   The sorting block 11 also receives at its input a request allocation signal PSgrn from a switching block 12, and it outputs to the switching block a sorting signal ORD of the power requests received from the plurality of modules Mod1, …, ModN. The switching block 12 receives, in turn, the power request signal Psreq. The switching block 12 is

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connected to the identification bus PSidfy which identifies the operation required, and to the priority bus Psrqpry. The switching block 12 provides, through the second bi-directional bus 6, the sorting block 11 and the plurality of memory modules Mod1, …, ModN with the request allocation signal PSgrn.

[0019]   The switching block 12 is also bi-directionally connected to a plurality of request decoders 13, to which it provides the power request signal Psreq, and from which it receives the request allocation signal PSgrn. The switching block 12 is also connected to the plurality of decoders 13 through the identification bus PSidfy.

[0020]   The plurality of request decoders 13 are connected in a multiplexed, bi-directional fashion to a plurality of driving circuits 14. The driving circuits 14, in turn, are connected through the first bi-directional bus 5 to the plurality of charge pump circuits Pump1, …, PumpM of the voltage generator block 3, to which they provide the following signals: the activation signal pump_pwd of a corresponding charge pump circuit; and a stand-by mode signal pump_stby of a corresponding charge pump circuit.

[0021]   The driving circuits 14 also receive from the plurality of charge pump circuits Pump1, …, PumpM a validity signal pump_valid. This signal provides the information that the charge pump has reached the desired value.

[0022]   It is possible to configure various functions using software. For example, such functions may include the correspondence between the type of operation required and the charge pumps needed to satisfy it,

power down and stand-by times, and the number of requests which can be satisfied by each charge pump at a given time.

[0023]   In accordance with the invention, the plurality of modules Mod0, …, ModN may advantageously be connected to the architecture 10 for distributing supply voltages. The same plurality of charge pump circuits Pmp1, …, PumpM may therefore be shared for generating the supply voltages Vhigh1, …, VhighN and Vneg1, …, VnegN needed for the correct operation of the modules themselves. The architecture 10 for distributing supply voltages, knowing how many operations may be supported by a predetermined charge pump circuit, may allow lower priority operations to wait until the corresponding charge pump circuits are free.

[0024]   Operation of the architecture 10 for distributing supply voltages according to the invention will now be described in greater detail. The sorting block 11 processes the voltage requests received from the plurality of modules Mod1, …, ModN on the basis of the following rules: request state (i.e., the request being already active or new request); priority information; and position of the module which has performed the request.

[0025]   The switching block 12 identifies the requests to be satisfied based upon the signal received from the sorting block 11. The switching block 12 spreads the corresponding signals to the plurality of request decoders 13, which in turn enable the corresponding driving circuits 14 of the charge pump circuits Pump1, …, PumpN. Particularly, driving

circuits 14 manage the power-down and stand-by conditions of the plurality of charge pump circuits Pump1, …, PumpM. The architecture 10 for distributing supply voltages thus provides for the scheduling of power requests received from the memory modules Mod1, …, ModN through a priority-scale-based sorting.

[0026]   In one exemplary implementation of the sorting block 11, a priority scale may be used in which reading operations are given priority with respect to programming operations, and programming operations are given priority with respect to erasing operations. Moreover, for the same operation, modules which are closer to the architecture 10 may be given priority with respect to further modules. For example, with reference to FIG. 1, the module Mod1 may be considered as the closest module and the module Mod4 the farthest from the architecture 10. In other words, the priority scale includes a priority classification of the different operations (i.e., reading, writing, and erasing) which can be performed on the memory cells of modules Mod1, …, Mod4, or of the requests received from the different modules.

[0027]   In addition, the architecture 10 may be implemented to sort the requests of the plurality of independent modules (Mod1, …, ModN) in a single cycle of the memory device 1 clock signal. By way of example, the clock signal may have a frequency of less than or equal to 250 MHz. It should also be noted that the delay introduced by the architecture 10 may be reduced to a single cycle of the memory device clock signal in some implementations.

[0028]   In conclusion, the architecture 10 for

distributing supply voltages according to the invention may be relatively easily implemented and has several advantages. First, it provides parallelism of the different operations (reading, writing, and erasing) performed on the memory cells of the different modules. Also, it allows several requests received from the modules to be managed by sorting them based upon a predetermined priority scale. Further, a relatively large number of modules to be managed may be connected to a same arbitrator, and the priority with which operations are to be managed may be software-reconfigured.